REMARKS

The specification has been amended to attend to minor matters. No new matter has been added.

Claims 5, 7 and 17 have been amended. Claims 1-8, 10-14 and 16-22 remain pending and under consideration, with claims 1, 14 and 20 being independent. Reconsideration and allowance of claims 1, 3-8, 10-14 and 16-22 is requested.

SECTION 112 REJECTIONS

Claims 5, 6, 13, and 15-17 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite. This contention is respectfully traversed. Please note that claim 15 was cancelled in the previous Amendment filed August 14, 2002. Also, claims 5 and 17 have been amended.

Claims 5, 6, 13 and 16-17, as presented, include one or more terms that are considered acceptable "relative terms" as described in various sections of MPEP § 2173.05(b). For example, MPEP § 2173.05(b)A describes the term "About" as an example of a clear, but flexible relative term (citing to *Ex parte Eastwood*, 163 USPQ 316, Bd. App. 1968). As another example, MPEP § 2173.05(b)D describes the term "Substantially" as an acceptable broad term that may be used to describe a particular characteristic of a claimed invention (citing *In re Nehrenberg*, 280 F.2d 161, 126 USPQ 383, CCPA 1960). Therefore, Applicants respectfully submit that claims 5, 6, 13 and 16-17 comply with the requirements of 35 U.S.C. § 112.

SECTION 102 AND 103 REJECTIONS

Claims 1, 3, 7, 8, 10, 14 and 16 are rejected under 35 U.S.C. §103(a) as being unpatentable over Boaz et al. [USPN 6,061,263] in view of Kumakura et al. [USPN 6,114,751] and alleged Applicant Admitted Prior Art (AAPA). Claims 4, 5, 11, 12,17 and 18 are rejected under 35 U.S.C. §103(a) as being unpatentable over Boaz et al. [USPN 6,061,263] in view of Kumakura et al. [USPN 6,114,751] and alleged Applicant Admitted Prior Art (AAPA) as applied to claim 1 above, and further in view of Perino et al. [USPN 6,160,716]. Claims 6, 13 and 19 are rejected under U.S.C. §103(a) as being unpatentable over Boaz et al. [USPN 6,061,263] in view of Kumakura et al. [USPN 6,114,751] and alleged Applicant Admitted Prior Art (AAPA) as applied to claim 1 above, and further in view of Holman et al. [USPN 6,005,776]. Claims 20 and 21 are rejected under 35 U.S.C. §103(a) as being unpatentable over Leddige et al. [USPN 6,111,205], in view of Kumakura et al. [USPN 6,114,751], alleged AAPA, and Boaz et al. [USPN 6,061,263].

The present invention describes routing signal lines between a memory control unit and a memory unit that does not require a ground trace line between the signal lines. See, for example, Figure 3 and the description at pages 3-5. The inventor found that a gap formed between neck down portions of each signal line provides an isolation between the signal lines yet reduces the area required to route the signal lines on a circuit board. Placing the gap, and not a ground trace, between the neck down portions may reduce congestion at the memory unit. This allows the signal lines into and out of the memory unit to be routed on a single layer of the circuit board on which the memory control unit (MCU) and the memory unit reside. Routing the signal lines in this manner may reduce the number of layers

required to route signals between the MCU and the memory unit by a factor of two. As a result, the circuit board on which the MCU and memory unit reside can be less expensive to produce than conventional memory boards.

Consider exemplary claim 1, which recites, in relevant part:

"a computer system comprising: a processor; a memory unit configured to store data used by the processor; a memory control unit configured to manage data flowing into and out of the memory unit; circuit board having multiple layers and comprising: a first signal line, formed on a first layer of the circuit board and connected between a first connection on the memory unit and the memory control unit; and a second signal line also formed on the first layer of the circuit board and connected to the first connection on the memory unit, a first portion of the second signal line substantially parallel to a first portion of the first signal line, a second portion of the second signal line at an acute angle relative to a second portion of the first signal line,
wherein said layer defines a non-grounded gap between said first and second lines."

The art of record fails to disclose or suggest the combination of features recited in independent claim 1.

In support of the rejection of claims 1, 3, 7, 8, 10, 14, 16 and 22 the Examiner states in item 5 of the office action that Boaz et al. discloses a "circuit board" having "multiple layers". However, this characterization of a "circuit board" is totally different than "a circuit board having multiple layers", as taught and claimed by the Applicants. To the contrary, in order to construct this alleged "circuit board" of Boaz et al., the Examiner requires that two separate boards,

i.e., motherboard 10 and RIMM board 17 be combined. In more detail, Boaz et al. discloses two boards that are connected through an edge connector 19, i.e., a motherboard 17 that includes a plurality of edge connectors 19, and a plurality of memory module boards 14 that are inserted (and connected) to each of the edge connectors 19. (col. 2, lines 36-57). Therefore, Boaz et al. cannot properly be characterized as describing "a circuit board having multiple layers" as required by applicants' claim 1.

The Examiner also states in item 5 of the office action that the Applicant has Admitted as Prior Art (AAPA) to "a portion of the signal line at an acute angle relative to a portion of another signal line". In support of this allegation, the Examiner makes reference to the relationship of signal lines 150 and 160 of Fig. 2 of the application. This characterization of what is admitted as prior art is respectfully traversed. Contrary to the Examiner's characterization, the Applicant clearly states on page 2, lines 7-10 of the application, that Fig. 2 merely shows a prior art system that includes a "signal line 150 [that] *narrows*, or "necks down", to a width of approximately 5 mils. The signal line 160 exiting the pin 155 also has a width of approximately 5 mils before *expanding* to a width of approximately 18 mils." That is, Fig. 2 shows the tapering of signal lines 150 and 160, and is further supported by the application which describes the signal lines 150 and 160 as *narrowing* and/or *expanding* to the connection point 155.

The Examiner also included a discussion of Kumakura et al. [USPN 6,114,751], Perino et al. [USPN 6,160,716], Holman et al. [USPN 6,005,776], and Leddige et al. [USPN 6,111,205], all in view of Boaz et al. [USPN 6,061,263] and alleged AAPA. For at least the reasons stated above with regard to Boaz et al. and

the alleged AAPA, none of the proposed combinations with the other prior art cited would anticipate or render obvious applicants' claims. Specifically, applicants' claim 1 recites: a "a memory unit ... a memory control unit... a circuit board having multiple layers and comprising: a first signal line, formed on a first layer of the circuit board and connected between a first connection on the memory unit and the memory control unit; and a second signal line also formed on the first layer of the circuit board and connected to the first connection on the memory unit, a first portion of the second signal line substantially parallel to a first portion of the first signal line, a second portion of the second signal line at an acute angle relative to a second portion of the first signal line, wherein said layer defines a non-grounded gap between said first and second lines."

With regard to the proposed combination of Kumakura et al.[USPN 6,114,751], Perino et al.[USPN 6,160,716], Holman et al.[USPN 6,005,776], and Leddige et al. [USPN 6,111,205], all in view of Boaz et al.[USPN 6,061,263] and alleged AAPA, it is well established that in order for any prior art references to be validly combined in a prior art 35 USC §103 rejection, the references themselves (or some other prior art) must suggest that they be combined (see MPEP §2143). In the present case, there is no reason given by the Examiner, and no reasons or suggestions found in the cited references, to support the proposed combinations. Applicants submit that the various proposed combinations of Kumakura et al.[USPN 6,114,751], Perino et al.[USPN 6,160,716], Holman et al.[USPN 6,005,776], and Leddige et al. [USPN 6,111,205], all in view of Boaz et al.[USPN 6,061,263] and alleged AAPA are improper and the rejection should be withdrawn.

Furthermore, the Examiner is directed to MPEP §2143, entitled "Basic Requirements of a *Prima Facie* Case of Obviousness":

> "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion of motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all of the limitations.
>
> The teaching or suggestion to make the claimed combination and the reasonable expectation of success must be found in the prior art, not in the applicants' disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)."

The Examiner simply has not provided any teaching or suggestion from the prior art to make any of the proposed combinations of Kumakura et al.[USPN 6,114,751], Perino et al.[USPN 6,160,716], Holman et al.[USPN 6,005,776], and Leddige et al. [USPN 6,111,205], all in view of Boaz et al.[USPN 6,061,263] and alleged AAPA. The rejection of claims 1, 3-8, 10-14 and 16-22 based on the proposed combinations of Kumakura et al.[USPN 6,114,751], Perino et al.[USPN 6,160,716], Holman et al.[USPN 6,005,776], and Leddige et al. [USPN 6,111,205], all in view of Boaz et al.[USPN 6,061,263] and alleged AAPA represents classic hindsight reconstruction, improperly using applicants' claims as a template to reconstruct the invention by picking and choosing isolated disclosures from the prior art.

This is impermissible as a matter of law.

For example, one of the cases cited in MPEP §2143.01 is in *In re Fine*, 837 F.2d at 1075, 5 USPQ2d at 1600. In *In re Fine*

the court said: "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." The present rejection fits the court's description of what may not be done under § 103. The Examiner has merely listed certain components of applicants' invention and then located isolated disclosures of those components in various different references. The law requires more than that.

Finally, even if arguendo the proposed combinations of Kumakura et al. [USPN 6,114,751], Perino et al. [USPN 6,160,716], Holman et al. [USPN 6,005,776], and Leddige et al. [USPN 6,111,205], all in view of Boaz et al. [USPN 6,061,263] and alleged AAPA were suggested, none of the proposed combinations would anticipate or render obvious applicants' claim 1.

Similarly, applicants' claim 14, recites "A method for use in manufacturing a computer system, the method comprising: forming a multiple-layer circuit board with first and second signal lines on a selected layer of the board; connecting a memory unit to the board such that a first connection on the memory unit connects to the first and second signal lines; affixing a memory control unit to the board such that the memory control unit connects to at least the first signal line; forming a first portion of the second signal line to be substantially parallel to a first portion of the first signal line; and forming a second portion of the second signal line to be at an acute angle relative to a second portion of the first signal line.." None of the prior art cited - - whether taken alone or in combination - - describe or suggest the features recited in applicants' claims 1 and 14, respectively.

Similarly, applicants' claim 20 recites: "A circuit board for use in a computer system comprising: a memory unit; a memory

control unit; and a data bus connecting the memory control unit to the memory unit and comprising: a first signal line formed on a selected layer of the circuit board and connected to the memory control unit and to a first connection on the memory unit; and a second signal line formed on the selected layer of the circuit board and also connected to the first connection on the memory control unit, a first portion of the second signal line substantially parallel to a first portion of the first signal line, a second portion of the second signal line at an acute angle relative to a second portion of the first signal line, wherein said selected layer defines a non-grounded gap between said first and second lines. None of the prior art cited - - whether taken alone or in combination - - describe or suggest the features recited in applicants' claims 1, 14, and 20, respectively.

Accordingly, claims 1, 14 and 20 are allowable for the reasons discussed above. The remaining claims each depend directly or indirectly from one of the independent claims discussed above. Accordingly, these dependent claims are allowable for the reasons that their respective independent claims are allowable and for reciting allowable subject matter in their own right. Independent consideration and allowance of the dependent claims are requested.

Attached is a marked-up version of the changes being made by the current amendment.

Attorney's Docket No.: 10559-108001 / P7643

Applicant asks that all claims be allowed. Please apply any other charges or credits to Deposit Account No. 06-1050.

Respectfully submitted,

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Jerry D. Lentz
Reg. No. 33,945

Fish & Richardson P.C.
PTO Customer No. 20985
4350 La Jolla Village Drive, Suite 500
San Diego, California 92122
Telephone: (858) 678-5070
Facsimile: (858) 678-5099
10232620.doc

Version with markings to show changes made

In the specification:

Paragraph beginning at page 1, line 19 has been amended as follows:

-- The speed at which the computer operates depends in large part on the speed at which data is transferred between the processor 105 and the memory unit 110. One memory architecture in particular, known as the RAMBUS™ [Rambus] architecture, is designed to transfer data to the processor 105 at very high rates, e.g., 1.6 GB/s for a typical RAMBUS™ [Rambus] DRAM (RDRAM) module. -

Paragraph beginning at page 5, line 11 has been amended as follows:

-- A number of embodiments have been described. Nevertheless, one of ordinary skill will understand that variations are possible. For example, while the invention has been described in terms of signal routing to a RAMBUS™ [Rambus] device, this scheme is useful in routing signals to other types of memory devices and even to other system components. Accordingly, other embodiments are within the scope of the following claims. -

In the claims:

Claims 5, 7 and 17 have been amended as follows:

5. (Twice Amended) The system of claim 4, wherein the first signal line and the portion of the second signal line that is routed substantially parallel to the first signal line are

separated by a distance about [approximately] equal to said widths.

7. (Amended) The system of claim 1, wherein the memory unit comprises a RAMBUS™ [Rambus] device.

17. (Twice Amended) The method of claim 16, further comprising forming the first signal line and the first portion of the second signal line that is routed substantially [roughly] parallel to the first signal line to have substantially equal widths.